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*Admitted only in Maryland *Admitted only in Virginia *Admitted only in Texas *Practice Limited to

August 29, 2002

WRITER'S DIRECT NUMBER:

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Commissioner for Patents Washington, D.C. 20231

Re:

U.S. Utility Patent Application

Appl. No. 10/020,207; Filed: December 18, 2001

Ball Grid Array Package Substrates and Method of Making the Same

Inventors: Khan et al. 1875.1640000 Our Ref:

Sir:

Transmitted herewith for appropriate action are the following documents:

- Information Disclosure Statement (IDS); 1.
- A listing of the cited documents on Form PTO-1449 (20 pages); 2.
- Copies of the one hundred five (105) documents listed on the PTO Form-1449; 3. and
- 4. One (1) return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

Commissioner for Patents August 29, 2002 Page 2

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jeffrey S. Weaver

Attorney for Applicants

July S. Wea

Registration No. 45,608

JSW/adw Enclosures

SKGF_DC1:50172.1





IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Khan et al.

Appl. No. 10/020,207

Filed: December 18, 2001

For: Ball Grid Array Package

Substrates and Method of Making

the Same

Confirmation No. 7969

Art Unit: 2811

Examiner: To be assigned

Atty. Docket: 1875.1640000

Information Disclosure Statement

Commissioner for Patents Washington, D.C. 20231

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Where the publication date of a listed document does not provide a month of publication, the year of publication of the listed document is sufficiently earlier than the effective U.S. filing date and any foreign priority date so that the month of publication is not in issue. Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.



This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

- 1. This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.
- □ 2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.
 - □ a. I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
 - □ b. I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

	□ c.	Attached is our Check No in the amount of \$ in payment
		of the fee under 37 C.F.R. § 1.17(p).
□ 3.	This I	nformation Disclosure Statement is being filed more than three months after
		the U.S. filing date and after the mailing date of a Final Rejection or Notice
		of Allowance, but before payment of the Issue Fee. Enclosed find our Check
		No in the amount of \$ in payment of the fee under 37
		C.F.R. § 1.17(p); in addition:
	□ a.	I hereby state that each item of information contained in this Information
		Disclosure Statement was cited in a communication from a foreign
		patent office in a counterpart foreign application not more than three
		months prior to the filing of this Information Disclosure Statement.
		37 C.F.R. § 1.97(e)(1).
	□ b.	I hereby state that no item of information in this Information Disclosure
		Statement was cited in a communication from a foreign patent office
		in a counterpart foreign application and, to my knowledge after
		making reasonable inquiry, was known to any individual designated
		in 37 C.F.R. § 1.56(c) more than three months prior to the filing of
		this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
□ 4 .	The d	ocument(s) was/were cited in a search report by a foreign patent office in a
		counterpart foreign application. Submission of an English language version
		of the search report that indicates the degree of relevance found by the
		foreign office is provided in satisfaction of the requirement for a concise
		explanation of relevance. 1138 OG 37, 38.
□ 5.	A cor	ncise explanation of the relevance of the non-English language document(s)
		appears below:
□ 6.	Copie	s of the documents were cited by or submitted to the Office in an IDS that
		complies with 37 C.F.R. § 1.98(a)-(c) in Application No, filed
		, which is relied upon for an earlier filing date under 35 U.S.C.
		§ 120. Thus, copies of these documents are not attached. 37 C.F.R.
		§ 1.98(d).



It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Ur S. Wer

Jeffrey S. Weaver

Attorney for Applicants Registration No. 45,608

Date: 8-29-02

1100 New York Avenue, N.W. Suite 600 Washington, D.C. 20005-3934 (202) 371-2600

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT PRADEM

ATTY. DOCKET NO. 1875.1640000

APPLICATION NO. 10/020,207

APPLICANT Khan et al.

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	AO	1	Amkor Electronics, "Amkor BGA Packaging: Taking The World By Storm", Electronic Packaging & Production, Cahners Publishing Company, May 1994, page unknown.								
	АР	1	Anderson, L. and Trabucco, B., "Solder Attachment Analysis of Plastic BGA Modules", Surface Mount International Conference, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 189-194.								
Andrews, M., "Trends in Ball Grid Array Technology," Ball Grid Array National March 29-30, 1995, Dallas, Texas, 10 pages.							National S	ymposium,			
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FORM PTO-1449

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APPLICANT: Khan *et al*.

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	AN	2	Banerji, K., "Development of the Slightly Larger Than IC Carrier (SLICC), Journal of Surface Mount Technology, July 1994, pp. 21-26.								
Bauer, C., Ph.D., "Partitioning and Die Selection Strategies for Cost Effective MCM Dournal of Surface Mount Technology, October 1994, pp. 4-9. Bernier, W.E. et al., "BGA vs. QFP: A Summary of Tradeoffs for Selection of High I/Components", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 181-185. Burgos, J. et al., "Achieving Accurate Thermal Characterization Using a CFD Code-Study of Plastic Packages", IEEE Transactions on Components, Packaging, and Man Technology Part A, IEEE, December 1995, Vol. 18, No. 4, pp. 732-738.							CM Designs",				
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conformance and not considered. Include copy of this form with next communication to Applicant.

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FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO. 1875.1640000

APPLICATION NO. 10/020,207

APPLICANT

Khan et al. FILING DATE

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2811 December 18, 2001 **U.S. PATENT DOCUMENTS EXAMINER** DOCUMENT CLASS SUB-FILING DATE INITIAL DATE NAME **CLASS** NUMBER AA3 AB3 AC3 AD3 AE3 AF3 AG3 AH3 AI3 **FOREIGN PATENT DOCUMENTS EXAMINER** CLASS TRANSLATION INITIAL DOCUMENT NUMBER DATE COUNTRY SUB-CLASS AJ3 Yes No Yes AK3 No Yes AL3 Nο AM3 Yes OTHER (Including Author, Title, Date, Pertinent Pages, etc.) Chanchani, R. et al., "Mini BGA: Pad and Pitch Ease Die Test and Handling", Advanced Packaging, IHS Publishing Group, May/June 1995, pp.34, 36-37. ΑN 3 Chung, T.C. et al., "Rework of Plastic, Ceramic, and Tape Ball Grid Array Assemblies", Ball Grid Array National Symposium Proceedings, Dallas, Texas, March 29-30, 1995, pp. 1-15. AO 3 Cole, M.S. and Caulfield, T. "A Review of Available Ball Grid Array (BGA) Packages", Journal of Surface Mount Technology, Surface Mount Technology Association, January 1996, Vol. 9, pp. 4-11. ΑP <u>3</u> Cole, M.S. and Caulfield, T., "Ball Grid Array Packaging", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 147-153. AQ <u>3</u> Dobers, M. and Seyffert, M., "Low Cost MCMs: BGAs Provide a Fine-Pitch Alternative", Advanced Packaging, IHS Publishing Group, September/October 1994, Vol. 3, No. 5, pp. 28, 30 AR 3 and 32. **EXAMINER** DATE CONSIDERED

AUG 2 9. 2002

FORM PTO-1449

INFORMATION	DISCLOSURE	STATEMENT

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ATTY. DOCKET NO. 1875.1640000	APPLICATION NO. 10/020,207
APPLICANT Khan et al.	
FILING DATE December 18, 2001	GROUP 2811

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	AO	<u>4</u>	Edwards, D. et al., "The Effect of Internal Package Delaminations on the Thermal Performance of PQFP, Thermally Enhanced PQFP, LOC and BGA Packages", 45th Electronic Components & Technology Conference, IEEE, May 21-24, 1995, Las Vegas, NV, pp. 285-292.								
	AP	4	Ejim, T.L. e Packages", January 199	t al., Jourr 96, Vo	"Designed lal of Surfa ol. 9, pp. 3	Expe ace M 0-38.	riment to Determine ount Technology, S	e Attachme urface Mou	ent Relia unt Tech	ability Drive	ers for PBGA sociation,
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ATTY. DOCKET NO. 1875.1640000	APPLICATION NO. 10/020,207
APPLICANT Khan et al.	
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AUG 2 9 2002

FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

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·	АР	<u>6</u>	Freyman, B Texas, Marc	., "Tre :h 29-	ends in Pla 30, 1995,	stic B 45 pa	GA Packaging," Ball (ages.	Grid Arra	y Natio	nal Sympo	sium, Dallas,	
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ATTY. DOCKET NO. 1875.1640000	APPLICATION NO. 10/020,207
APPLICANT Khan et al.	
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	AR	7	Hodson, T. unknown.	, "Stu	dy Examir	nes BO	GA Use", Electronic I	Packagin	g & Prod	luction, Ma	rch 1993, page	
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ATTY. DOCKET NO. 1875.1640000	APPLICATION NO. 10/020,207
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	AN	<u>8</u>	Holden, H. Interconne Diego, CA,	Holden, H., "The Many Techniques of Small Via Formation for Thin Boards", The Institute for Interconnecting and Packaging Electronic Circuits Ball Grid Array National Symposium, San Diego, CA, January 18-19, 1996, pp. 1-7.									
	AO	<u>8</u>	Houghten, Winter 199	Houghten, J., "New Package Takes On QFPs", Advanced Packaging, IHS Publishing Group, Winter 1993, Vol. 2, No. 1, pp. 38-39.									
	АР	<u>8</u>	"How To G January/Fe	ive Yo bruar	our BGAs A y 1995, pa	Bett ge u	er Bottom Line.", Ad nknown.	dvanced Packagi	ng, IHS Pub	olishing Group,			
	AQ	<u>8</u>	Huang, W. by Simulati West '95, F	and fon an	Ricks, J.,"El nd Measure ary 26-Marc	ectri ment ch 2,	cal Characterization ", National Electron 1995, Anaheim, Cal	of PBGA for Cor ic Packaging and lifornia, pp. 300-	nmunication Production 307.	n Applications n Conference			
	AR	<u>8</u>	Hundt, M. (and Produc 29, 1996, p	et al., etion (pp. 70	"Thermal Conference 2-711.	Enha Wes	ncements of Ball Gr t '95, Reed Exhibitio	id Arrays", Natio on Companies, A	nal Electror naheim, CA	nic Packaging , February 25-			
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	AN	9	Hutchins, C Publishing C	.L., "L Group,	Inderstand , Novembe	ling G er 199	irid Array Packages", 14, Vol. 8, No. 11, pp	, Surfac o. 12-13	e Mount 3.	Technology	y Magazine, IHS	
	AO	<u>9</u>	Hwang, J.S. IHS Publishi	, "Rel Ing Gr	iability of I oup, Septe	BGA Solder Interconnections", Surface Mount Technology Magazine, ember 1994, Vol. 8, No. 9, pp. 14-15.						
	AP	9	Hwang, J.S. IHS Publish	Hwang, J.S., "A Hybrid of QFP and BGA Architectures", Surface Mount Technology Magazine, IHS Publishing Group, February 1995, Vol. 9, No. 2, p. 18.								
	AQ	9	Johnson, R. Packaging a 413-422.	Johnson, R. et al., "A Feasibility Study of of Ball Grid Array Packaging", National Electronic Packaging and Production Conference East '93, Boston, Massachusetts, June 14-17, 1993, pp. 413-422.								
	AR	9	I National Ele	Johnson, R. et al., "Thermal Characterization of 140 and 225 Pin Ball Grid Array Packages", National Electronic Packaging & Production Conference East '93, Boston, Massachusetts, June 14-17, 1993, pp. 423-430.								
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	AN	<u>10</u>	Johnston, Dallas, Tex	P., "La cas, M	and Patter arch 29-30	n Inte 0, 199	erconnectivity Schem 15, pages 2-21.	es", I	Ball Grid Arr	ay Nationa	l Symposium,
	AO	<u>10</u>	Johnston, Surface Mo 12-18.	P. "Pr ount T	inted Circu echnology	it Boa , Suri	ard Design Guideline ace Mount Technolo	s for logy As	Ball Grid Arssociation,	ray Packag January 19	es", Journal of 96, Vol. 9, pp.
	АР	<u>10</u>		is of t	he 1995 Ir	nterna	rray Type Package B Itional Electronics Pa 7-587.				
	AQ	<u>10</u>	Knickerboo Packaging,	ker, J IHS	.U. and Co Publishing	ole, M Grou _l	.S., "Ceramic BGA: / o, January/February	A Pac 1995	kaging Alte , Vol. 4, No	rnative", Ao . 1, pp. 20,	dvanced 22 and 25.
-	AR	<u>10</u>	I Microproce	ssor".	. National I	Electr	ty C4/CBGA Intercon onic Packaging and I sheim, California, pp.	Produ	iction Confe	for a CMC erence Wes	PS t '95, IEEE,
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	AN	<u>11</u>	Kunkle, R., Texas, Mare	"Disc ch 29	rete Wiring -30, 1995,	g for . 9 pa	Array Packages", I ges.	Ball Grid	Array Nati	onal Sympo	osium, Dallas,	
	AO	<u>11</u>	Lall, B. et a Component 18, No. 4, p	l, "Me s, Pac p. 75	ethodology ckaging, a 8-764.	for T	hermal Evaluation anufacturing Tech	n of Mult nology P	ichip Modu Part A, IEEE	iles", IEEE ⁻ E, Decembe	Transactions on r 1995, Vol.	
	АР	<u>11</u>	Lasance, C. Independer Manufactur Technology	et al nt Cor ing To Socie	., "Therma npact Mod echnology ety, Decen	l Cha lels", Part inber	racterization of El IEEE Transactions A, IEEE Componei 1995, Vol. 18, No.	ectronic s on Com nts, Pack 4, pp. 7	Devices winponents, Foraging, and 23-731.	ith Boundar Packaging, a I Manufactu	y Condition and uring	
	AQ	<u>11</u>	Lau, J., "Ba	Lau, J., "Ball Grid Array Technology", McGraw-Hill Inc., 1995, entire book submitted.								
	AR	<u>11</u>	Lau, J. et al Wela Public	., "No ations	o Clean Ma s Ltd., Vol.	ass Re . 20, I	flow of Large Plas No. 3, March 1994	stic Ball (l, pp.15-	Grid Array 22.	Packages",	Circuit World,	
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	AN	<u>12</u>	"Literature Cahners Pu	'Literature Review", Special Supplement to Electronic Packaging & Production, February 1995, Cahners Publication, 10 pages.							
	АО	<u>12</u>	LSI LOGIC I document s	SI LOGIC Package Selector Guide, Second Edition, LSI Logic Corporation, 1994-1995, entire document submitted.							
	AP	<u>12</u>	"LTCC MCMs Lead to Ceramic BGAs," Advanced Packaging, IHS Publishing Group, September/October 1994, Vol. 3, No. 5, pp. 14-15.						ıp,		
	AQ	<u>12</u>	Mak, Dr. W. Finite Eleme October 199	.C. et ent M 94, pr	al., "Incre odeling", J p. 33-41.	eased lourn	SOIC Power Dissipa al of Surface Mount	ation Ca Techno	pability T logy, Suri	nrough Boa face Mount	ard Design and International,
	AR	<u>12</u>	Marrs, R.C. Advanced P 50, and 52.	and (ackag	Olachea, G ging, IHS F	i., "B(Publis	GAs For MCMs: Chai hing Group, Septen	nging Manber/Oct	arkets and ober 199	d Product F 4, Vol. 3, N	Functionality", lo. 5, pp. 48,
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	AO	<u>13</u>	Mawer, A. o Internation 1994, San	Mawer, A. et al., "Plastic BGA Solder Joint Reliability Considerations", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 239-251.							
	АР	<u>13</u>	Mazzullo, T Technology	Mazzullo, T. and Schaertl, L., "How IC Packages Affect PCB Design", Surface Mount Technology Magazine, February 1995, Vol. 9, No. 2, pp. 114-116.							
	AQ	<u>13</u>	Mearig, J., and Produc 295-299.	"An C	verview of Conference	f Man Wes	ufacturing BGA Tec t '95, February 26-N	thnology March 2	/", Nation , 1995, Ai	al Electroni naheim, Ca	ic Packaging lifornia, pp.
	AR	<u>13</u>	Mertol, A., Grid Array I Technology	'Appl Packa Part	ication of t ges", IEEE B: Advan	the Ta Tran ced P	aguchi Method on th isactions on Compo ackaging, IEEE, Nov	he Robu nents, F vember	ist Design Packaging 1995, Vo	of Molded , and Manu l. 18, No. 4	225 Plastic Ball Ifacturing I, pp. 734-743.
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	AN	Mescher, P. and Phelan, G., "A Practical Comparison of Surface Mount Assa Array Components", Surface Mount International Conference Proceedings, International, August 28-September1, 1994, San Jose, California, pp. 164-						nt Assembly dings, Surfa . 164-168.	/ for Ball Grid ace Mount		
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	АР	<u>14</u>	Olachoa G. "Managing Hoat: A Focus on Power IC Packaging". Floctronic Packaging 8.						ishing Group,		
	AQ	<u>14</u>							kaging & 4, pp. 26-28.		
	AR	<u>14</u>	"Pad Array Company,	Impro May 1	oves Densi 992, pp. 2	ty", E 5-26.	lectronic Packaging 8	& Product	ion, Ca	ahners Publ	ishing
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	AN	<u>15</u>	Partridge, 1 Journal of 15-20.	l. and Surfac	Viswanad ce Mount 1	ham, Fechn	P., "Organic Carrie ology, Surface Mou	r Requ Int Te	uirements fo chnology As	or Flip Chip sociation, I	Assemblies", July 1994, pp.
	AO	<u>15</u>	Ramirez, C Array", Sur August 28-	. and face N Septe	Fauser, S. Mount Inte mber1, 19	, "Fat ernatio 194, S	igue Life Comparisc onal Conference Pro an Jose, California,	on of oceedi	The Perimet ngs, Surface 58-266.	er and Full e Mount In	Plastic Ball Grid ternational,
	АР	<u>15</u>	Rogren, P., Production	"MCI Confe	M-L Built o erence We	n Ball st '94	Grid Array Format , Anaheim, Californ	s", Na iia, pp	tional Electr . 1277-1282	onic Packa	ging and
	AQ	<u>15</u>	Rooks, S., Internation California,	'X-Ra al, Pro op. 19	y Inspection oceedings 95-202.	on of of Th	Flip Chip Attach Usi e Technical Prograi	ing Di m, Au	gital Tomos gust 28-Sep	ynthesis", S tember1, 1	Surface Mount 994, San Jose,
	AR	<u>15</u>	Rukavina, I Symposium	I., "At i, Dall	tachment las, Texas,	Metho Marc	odologies: Ball Grid h 29-30, 1995, 37	Array pages	Technology	/", Ball Grid	l Array National
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	AN	<u>16</u>	Sack, T., ": 29-30, 199	Inspec 95, pag	tion Techr Jes 1-41.	nology	r", Ball Grid Array N	ational Symposiu	ım, Dallas,	Texas, March
	AO	<u>16</u>	Sakaguchi,	. Н., "Е	3GA Mount	tingTe	chnology," pgs. 1-4	1, date and sourc	e unknown	
	АР	<u>16</u>	Schmolze, Packaging	C. and & Prod	l Fraser, A duction, Ja	, "SP inuary	ICE Modeling Helps 1995, pp. 50-52.	Enhance BGA Pe	erformance	", Electronic
	AQ	<u>16</u>	Semicondu document	ıctor G submi	roup Pack tted.	age C	outlines Reference (Guide, Texas Inst	ruments, 1	995, entire
	AR	<u>16</u>	Shimizu, J. Jose, Califo	, "Plas ornia, <i>i</i>	itic Ball Gri August 31-	id Arr -Septe	ay Coplanrity", Surf ember 2, 1993, pp.	ace Mount Interr 86-91.	national Cor	nference, San
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	AN	<u>17</u>	Sigliano, R. Advanced i	, "Usi Packa	ing BGA Pa ging, IHS I	ickag Publis	es: An Appealing Te hing Group, March/	chno April	logy in a QF 1994, pp. 36	P and Fine 5-39.	-Pitch Market",
	AO	<u>17</u>	Sirois, L., " Advanced F	Dispe Packa	nsing for E ging, IHS I	BGA: / Publis	Automated Liquid Di hing Group, May/Jui	spen: ne 19	sing in a Hig 995, pp. 38 a	h-Density and 41.	Environment",
	АР	<u>17</u>	Solberg, V. Surface Fin Texas, Mar	, "Into ish oo ch 29	erconnection SMT Asso 3-30, 1995,	on St embly 10 p	ructure Preparation: Process Yield", Ball ages.	Imp Grid	oact of Mate Array Natio	rial Handlir nal Sympo	ng and PCB sium, Dallas
	AQ	<u>17</u>	"Survival of unknown.	f the I	Fittest", Ac	Ivanc	ed Packaging, IHS P	ublis	hing Group,	March/Apr	il 1995, page
	AR	<u>17</u>	Tuck, J., "E 24, 26, and	GA T I 28.	echnology	Bran	ches Out", Circuits A	\ssen	nbly, Februa	ry 1995, V	ol. 6, No. 2, pp.
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